(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 282 343 A1

(12) EUROPEAN PATENT APPLICATION
published in accordance with Art. 158(3) EPC

(43) Date of publication:
05.02.2003 Bulletin 2003/06

(21) Application number: 00976308.7

(22) Date of filing: 16.11.2000

(51) Int Cl.[7]: H05K 3/46

(86) International application number:
PCT/JP00/08105

(87) International publication number:
WO 01/087024 (15.11.2001 Gazette 2001/46)

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR

(30) Priority: 10.05.2000 JP 2000137144

(71) Applicant: Ibiden Co., Ltd.
Ogaki-shi, Gifu 503-0917 (JP)

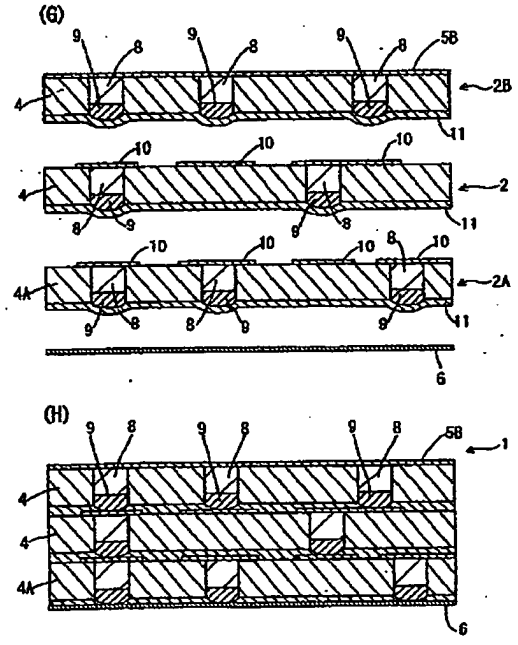
(72) Inventor: KARIYA, Takashi,
Tech. Res. Group, R & D Operation
Ibi-gun, Gifu 501-0695 (JP)

(74) Representative: Müller-Boré & Partner
Patentanwälte
Grafinger Strasse 2
81671 München (DE)

(54) METHOD OF PRODUCING MULTILAYER CIRCUIT BOARDS

(57) A plurality of printed boards is stacked and collectively pressed to be manufactured into a multilayer circuit board. An outermost conductor layer is stacked on an insulating layer side of a first outermost printed board disposed with the insulating layer side being directed outward, and pressed. A conductor layer of a second outermost printed board disposed with the conductor layer side being directed outward is previously formed with no conductor circuit and pressed under a condition where the conductor layer has a uniform thickness all over. Consequently, manufacturing steps can be simplified and the precision of the multilayer circuit board can be improved.

FIG. 2



EP 1 282 343 A1

Description

TECHNICAL FIELD

[0001] The present invention relates to a method of manufacturing a multilayer circuit board.

BACKGROUND ART

[0002] The build-up process is well known as a conventional method of manufacturing a multilayer circuit board. For example, a multilayer circuit board is manufactured as follows in this process. Firstly, via holes are formed at prescribed positions in a one-side copper-clad laminate manufactured by applying a copper foil to one side of an insulating substrate. The via holes are filled with an electrically conductive paste. A copper foil is bonded to the insulating substrate side of the one-side copper-clad laminate by pressing. The copper foil is etched so that a prescribed conductor circuit is formed.

[0003] A both printed board manufactured as described above serves as a core board. Insulating substrates are stacked on both sides of the core board respectively and bonded by pressing. Thereafter, via holes are formed at prescribed positions and then filled with the conductive paste. After copper foils are stacked on both sides of the board and pressed again, prescribed conductor circuits are formed on each copper foil. This step is repeated for further increase in the layers so that a multilayer circuit board is manufactured.

[0004] In the foregoing method, the both printed board serving as the core board is manufactured and circuit patterns are sequentially stacked on the core board. Accordingly, since the number of steps is increased, there is a definite limit in improvement of the manufacturing efficiency.

[0005] Furthermore, manufacture of the core board requires a step of bonding a copper foil by pressing in the conventional method. The pressing sometimes distorts the insulating substrate of the core board, whereupon positions of the via holes formed in the insulating substrate are sometimes displaced. Accordingly, a land needs to be rendered larger in consideration of allowance for displacement. This results in a problem that densification of the multilayer circuit board is difficult.

[0006] Additionally, when the insulating substrates are stacked on the core board, the pressing sometimes causes misregistration between the core substrate and each insulating board. Accordingly, an X-ray check hole needs to be previously formed so that the location of the inner conductor circuit is checked from the surface of the insulating board. This necessitates one extra step in the manufacture.

DISCLOSURE OF THE INVENTION

[0007] A first invention is a method of manufacturing a multilayer circuit board, in which a plurality of printed boards is stacked and pressed into a multilayer circuit board, each printed board having a conductor layer on one side of an insulating layer, characterized by the steps of stacking the printed boards with a bonding layer being interposed between the printed boards, and stacking an outermost conductor layer on an insulating layer side of a first outermost printed board with a bonding layer being interposed therebetween and pressing a stack so that the printed boards and the outermost conductor layer are bonded together, the first outermost printed board being disposed with the insulating layer side being directed outward.

[0008] A second invention is characterized in that the printed boards include a second outermost printed board disposed with a conductor layer side being directed outward, the conductor layer being pressed under a condition where the conductor layer has a uniform thickness all over.

[0009] According to the first invention, the printed boards each of which has one side formed with a conductor layer are stacked. The outermost conductor layer is stacked on the insulating layer side of the first outermost printed board disposed with the insulating layer side being directed outward. The printed boards are collectively pressed to be manufactured into a multilayer circuit board. Accordingly, the multilayer circuit board is manufactured by a single pressing operation. Consequently, the manufacturing steps can be simplified and the manufacturing efficiency can be improved.

[0010] Furthermore, since pressing is carried out just once, the possibility that the insulating substrate may be distorted and the possibility that the printed board may be shifted can be rendered minimum. Consequently, the precision of the multilayer circuit board can be improved.

[0011] According to the second invention, the second outermost printed board is not previously etched and pressed under the condition where the thickness thereof is entirely uniform. Accordingly, since a uniform pressure is applied to the whole printed board in the pressing, the possibility of distortion and displacement can be rendered minimum. Consequently, the precision of the multilayer circuit board can be improved.

BIREF DESCRIPTION OF THE DRAWINGS

[0012]

FIG. 1 is a sectional view (1) showing steps of manufacturing a multilayer circuit board of one embodiment in accordance with the present invention;
FIG. 2 is a sectional view (2) showing steps of manufacturing a multilayer circuit board of the embodiment in accordance with the present invention; and
FIG. 3 is a sectional view (3) showing steps of manufacturing a multilayer circuit board of the embodiment in accordance with the present invention.

BEST MODE FOR ENFORCEMENT OF THE INVENTION

[0013] One embodiment of the present invention will be described with reference to FIGS. 1 to 3.

[0014] In the method of manufacturing the multilayer circuit board 1 in accordance with the present invention, a plurality printed board 2 are stacked and collectively pressed. The method is characterized by stacking an outermost copper foil 6 (corresponding to an outermost conductor layer of the present invention) on a side of a first outermost printed board 2A at an insulating substrate 4A side and pressing, the printed board 2A having an insulating substrate 4 (corresponding to an insulating layer in the present invention) side being directed outward. See FIG. 2(G).

[0015] The method is further characterized in that a copper foil 5B of a second outermost printed board 2B disposed with the copper foil 5B (corresponding to a conductor layer in the present invention) side being directed outward is not previously formed with a conductor circuit 10 and is pressed under a condition where the copper foil 5B remains on the whole side.

[0016] The manufacture of the printed board 2 forming the multilayer circuit board 1 starts with a one-side copper-clad laminate 3. The one-side copper-clad laminate 3 has a well known structure, that is, the copper foil 5 is affixed to overall one side of an insulating substrate 4 (the underside in FIG. 1) made of a plate-shaped glass-cloth epoxy resin (FIG. 1(A)).

[0017] Laser beams are irradiated onto prescribed locations on the insulating substrate 4 from the side of the substrate opposite the copper foil 5 (the upper side in FIG. 1) so that via holes 7 extending through the insulating substrate to the copper foil 5 are formed (FIG. 1 (B)). The laser beam machining is executed by a pulse oscillation CO_2 gas laser, for example. In this case, the pulse energy preferably ranges between 2.0 and 10.0 mJ, the pulse width preferably ranges between 1 and 100 μs, the pulse interval is preferably at or above 0.5 ms, and the number of shots preferably ranges between 3 and 50.

[0018] Thereafter, desmearing is carried out in order that resin remaining in the via holes 7 may be removed. The desmearing includes a treatment of potassium permanganate, oxygen plasma discharge, corona discharge process, etc.

[0019] Subsequently, the copper foil 5 is covered with a protecting film made from polyethylene terephthalate although this state is not shown. In this state, a plated conductor 8 is formed in each via hole 7 by an electroplating with the copper foil 5 serving as one of electrodes (FIG. 1 (C)) . An amount of conductor 8 filling each via hole 7 is preferably determined so that an upper face thereof is slightly lower than the surface of the insulating substrate 4. Copper is most preferably as a plated metal but may be any metal which can be plated, such as tin, silver, solder, alloy of copper and tin, alloy of copper and silver, etc.

[0020] An electrically conductive bump 9 comprising a material with a low melting point, such as tin is formed by means of bump plating so that the bump overlaps the plated conductor 8 in each via hole 7. Each conductive bump 9 is formed so as to project slightly from the upper surface of the insulating substrate 4 (FIG. 1 (D)) . Subsequently, the copper foil 5 is etched so that a conductor circuit 10 is formed after the protecting film is stripped from the copper foil 5 (FIG. 1(E)).

[0021] A thermosetting adhesive (epoxy resin adhesive, for example) is applied by roll coating to the side of the printed board 2 on which the conductive bumps 9 are formed, whereby an adhesive layer 11 is formed (FIG. 1(F)).

[0022] A plurality of printed boards 2 manufactured as described above are aligned and overlapped (FIG. 2G). A second outermost printed board 2B of the top layer is overlapped without being etched. Accordingly, the copper foil 58 remains on the pranted board 2B with a uniform thickness over the whole surface. The printed board 2B is disposed so that the copper foil 5B is directed outward (upward in FIG. 2) and the conductive bumps 9 are directed inward. The printed board 2 located below the printed board 2B is stacked so that the conductor circuits 10 are positioned at the upper side of the printed board 2. Thus, the printed boards are stacked so that the conductive bumps 9 of the printed board 2 located upward are connectable to the conductor circuits 10 of the lower printed board 2. Additionally, a first outermost printed board 2A located lowermost is stacked so that the insulating substrate 4A side formed with the adhesive layer 11 is directed outward (downward in FIG. 2). An outermost copper foil 6 is stacked on the surface of the printed board 2A.

[0023] The printed boards thus stacked are heated and pressed under vacuum at 180°C for 70 minutes so that the adhesive layer 11 is hardened, whereby the printed boards 2, 2A and 2B, and the outermost copper foil 6 are bonded together. The multilayer circuit board 1 in which the printed boards 2, 2A and 2B and outermost copper foil 6 are integrated is manufactured by one pressing operation (FIG. 2(H)). The distal ends of the conductive bumps 9 of each printed board are connected to prescribed locations of the conductor circuit 10 on the adjacent printed board 2, whereupon the conductor circuits 10 of the adjacent printed boards 2 are electrically connected to each other.

[0024] Subsequently, the copper foil 5B on the uppermost side and the outermost copper foil 6 affixed to the underside are etched so that conductor circuits 10 are formed (FIG. 3(I)).

[0025] A photosensitive solder resist 12 is applied to the whole underside and exposure and development processes are applied to the solder resist in a prescribed pattern so that the solder resist 12 is formed with openings which open lands formed at prescribed locations on the conductor circuit 10. Pins 13 for connecting the

multilayer circuit board 1 to other components are bonded to the lands by solder 14. The multilayer circuit board 1 is thus manufactured.

[0026] According to the foregoing embodiment, the multilayer circuit board 1 is manufactured by stacking a plurality of printed boards 2 and stacking the outermost copper foil 6 on the insulating substrate 4A side of the first outermost printed board 2A disposed with the insulating substrate side being directed outward, and collectively pressing the stack. Accordingly, the multilayer circuit board 1 can be manufactured by a single time of pressing. Consequently, manufacturing steps can be simplified and the precision of the multilayer circuit board can be improved.

[0027] Furthermore, since pressing is carried out just once, the possibility that the insulating substrate 4 and the via holes 7 may be displaced can be rendered minimum. Consequently, the precision of the multilayer circuit board can be improved.

[0028] Furthermore, the copper foil 5B of the second outermost printed board 2B disposed with the copper foil side being directed outward is not previously etched, and the printed board 2B is pressed under the condition where the copper foil 5B having a uniform thickness all over is present. Accordingly, a uniform pressure can be applied to the whole printed board 2 and accordingly, the possibility that inner printed board 2 may be shifted or distorted can be rendered minimum. Consequently, the precision of the multilayer circuit board 1 can be improved.

[0029] The method of manufacturing the multilayer circuit board 1 can be applied to the manufacture of packages required of a particularly high precision. The underside on which the pins 13 are provided is preferably the outermost copper foil 6 side. The precision required for the lower layer side is lower than the precision required for the upper layer side and accordingly, the precision does not result in a problem even if the outermost copper foil 6 is stacked on the lowermost layer and pressed.

[0030] The technical scope of the present invention should not be limited by the above-described embodiment and covers equivalents thereof.

INDUSTRIAL APPLICABILITY

[0031] The present invention can provided a method of manufacturing a multilayer circuit board which can simplify the manufacturing steps and improve the precision of the multilayer circuit board.

Claims

1. A method of manufacturing a multilayer circuit board, in which a plurality of printed boards is stacked and pressed into a multilayer circuit board, each printed board having a conductor layer on one side of an insulating layer, **characterized by** the steps of stacking the printed boards with a bonding layer being interposed between the printed boards, and stacking an outermost conductor layer on an insulating layer side of a first outermost printed board with a bonding layer being interposed therebetween and pressing a stack so that the printed boards and the outermost conductor layer are bonded together, the first outermost printed board being disposed with the insulating layer side being directed outward.

2. A method of manufacturing according to claim 1, **characterized in that** the printed boards include a second outermost printed board disposed with a conductor layer side being directed outward, the conductor layer being pressed under a condition where the conductor layer has a uniform thickness all over.

FIG. 1

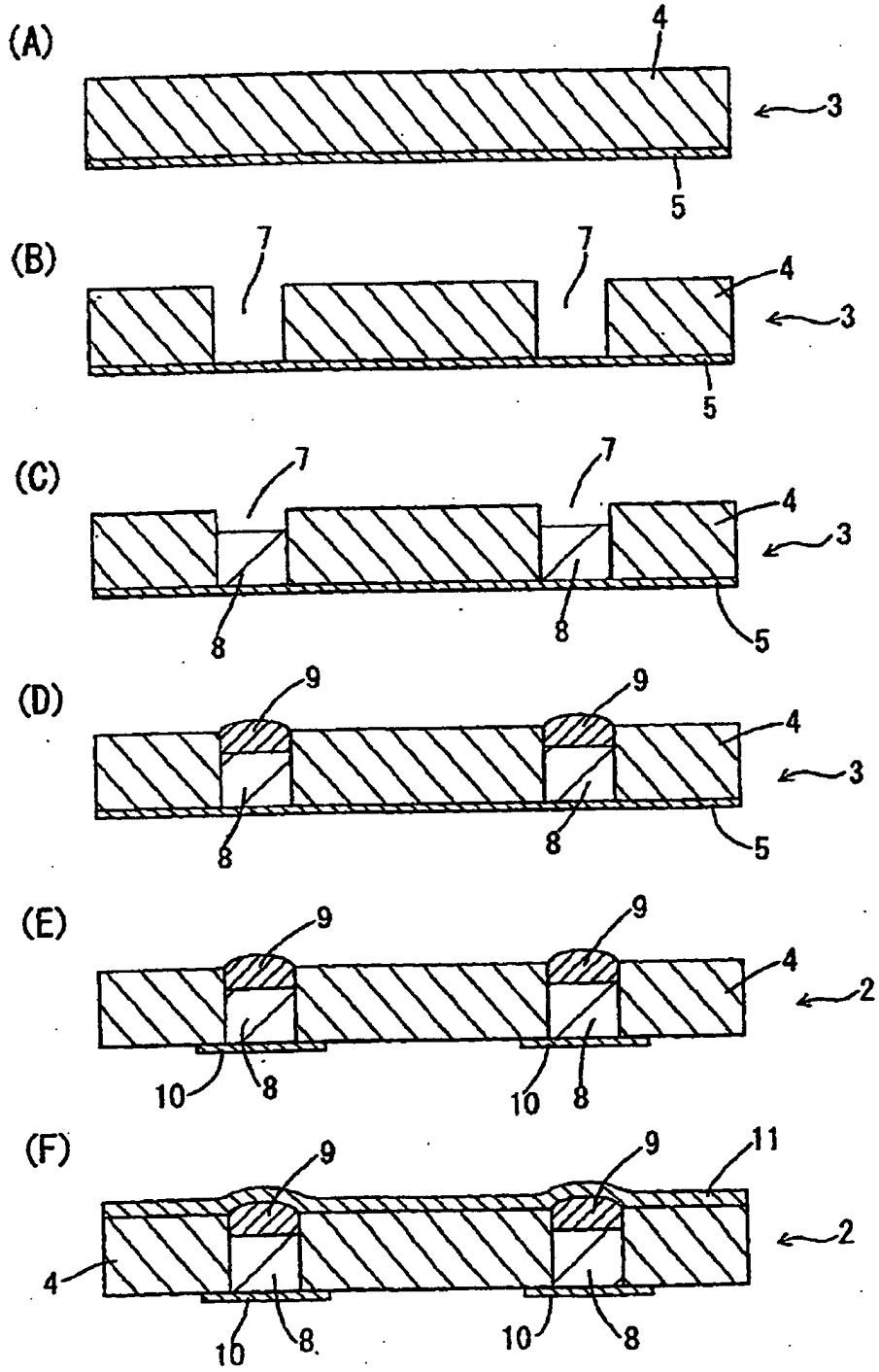

(A)
4
3
5
(B)
7
7
4
3
5
(C)
7
7
4
3
8
8
5
(D)
9
9
4
3
8
8
5
(E)
9
9
4
2
10
8
10
8
(F)
9
9
11
2
4
10
8
10
8

FIG. 2

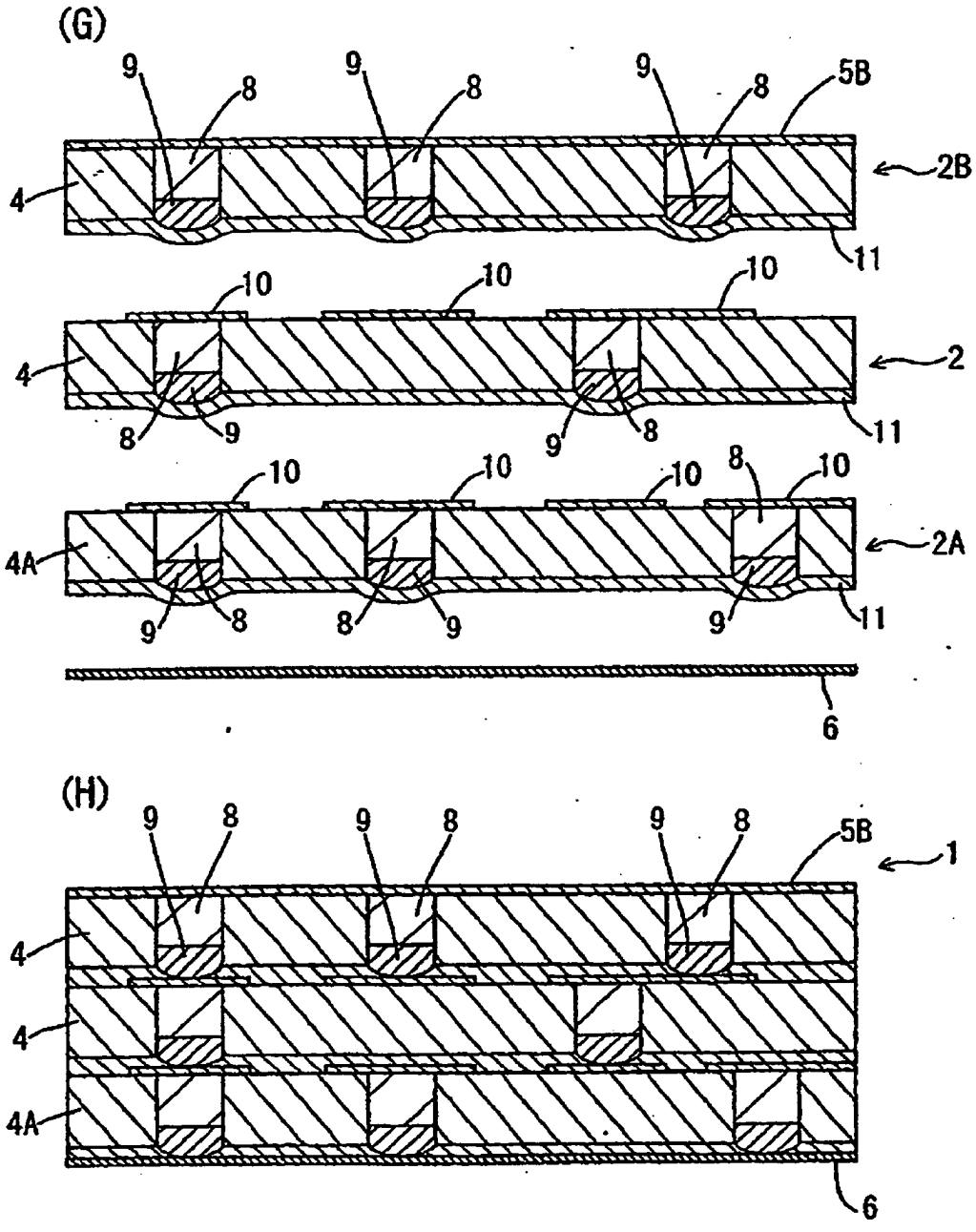
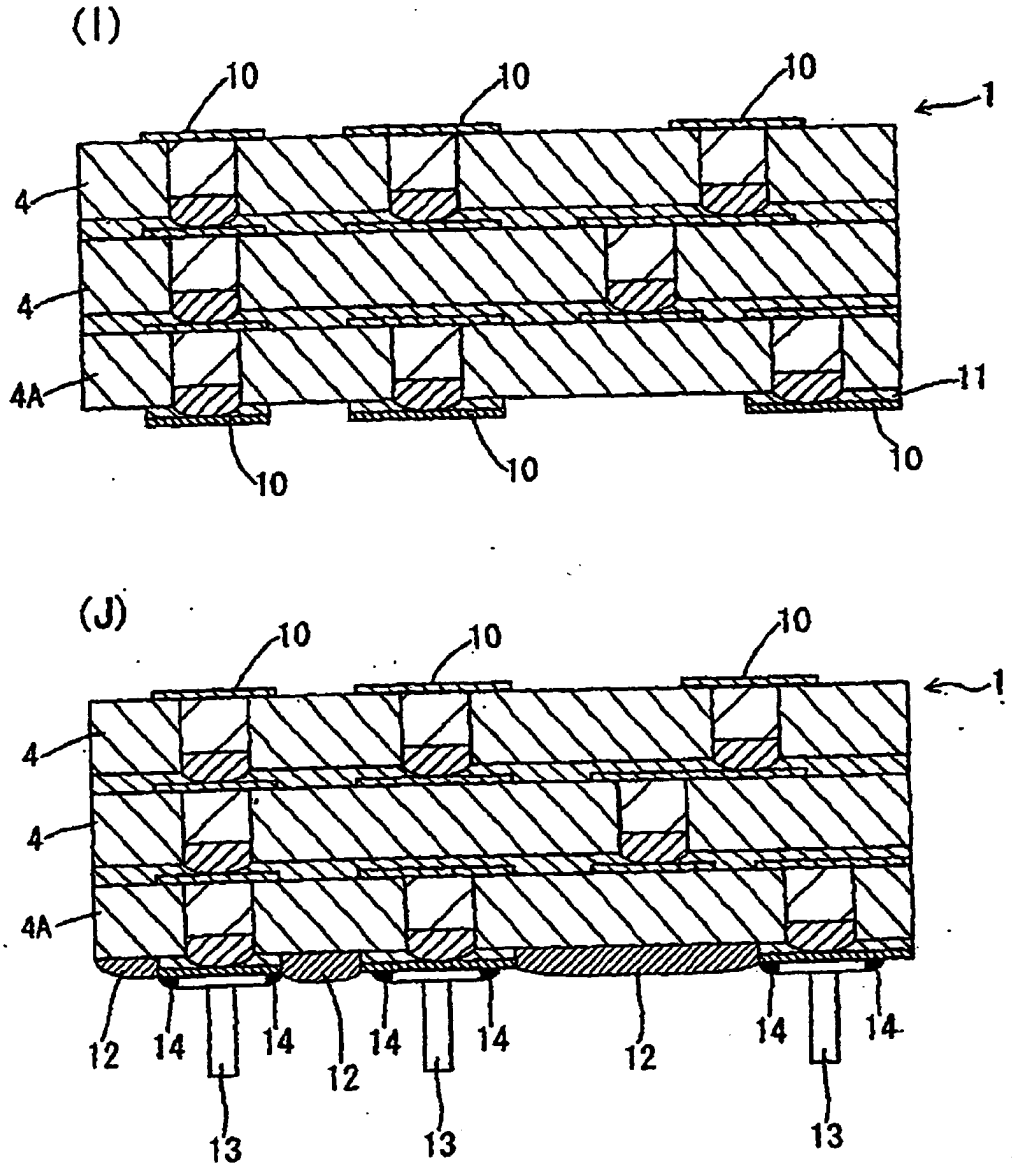


FIG. 3


(I)
10
10
10
1
4
4
4A
11
10
10
10
(J)
10
10
10
1
4
4
4A
12
14
14
12
14
14
12
14
14
13
13
13

INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/08105

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H05K3/46

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H05K3/46

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1926-1996 Jitsuyo Shinan Toroku Koho 1996-2001
Kokai Jitsuyo Shinan Koho 1971-2001 Toroku Jitsuyo Shinan Koho 1994-2001

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	JP, 4-10696, A (Nitto Denko Corporation), 14 January, 1992 (14.01.92) (Family: none)	1,2
Y	JP, 11-261225, A (Hitachi Cable, Ltd.), 24 September, 1999 (24.09.99) (Family: none)	1,2

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:
"A" document defining the general state of the art which is not considered to be of particular relevance
"E" earlier document but published on or after the international filing date
"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)
"O" document referring to an oral disclosure, use, exhibition or other means
"P" document published prior to the international filing date but later than the priority date claimed
"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
01 February, 2001 (01.02.01)	13 February, 2001 (13.02.01)
Name and mailing address of the ISA/ Japanese Patent Office	Authorized officer
Facsimile No.	Telephone No.

Form PCT/ISA/210 (second sheet) (July 1992)